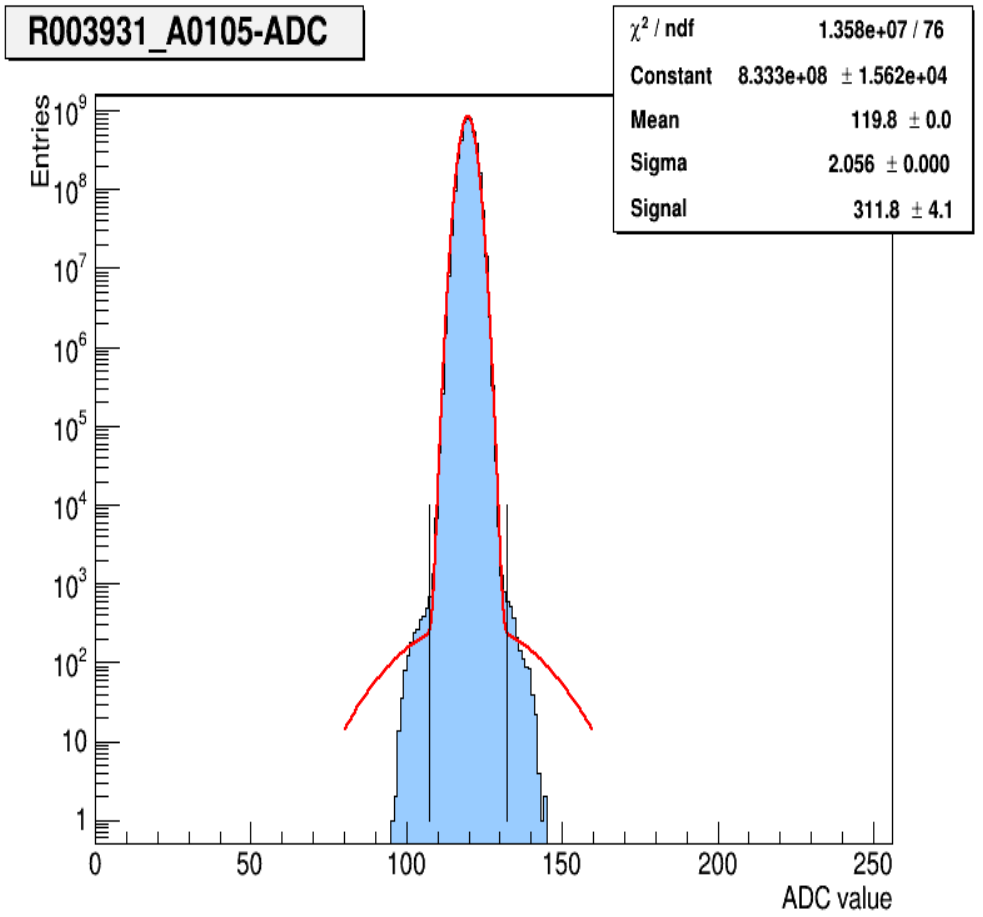
Comments on Trend DAQ

- 8 bit ADC range
- Clock distribution over fiber
- Digital threshold comparism

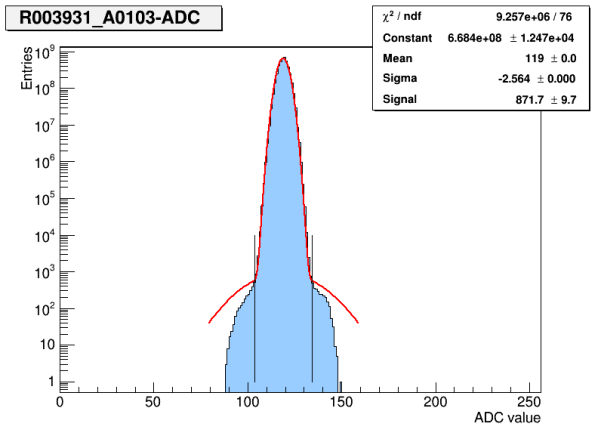
Michael Schernau

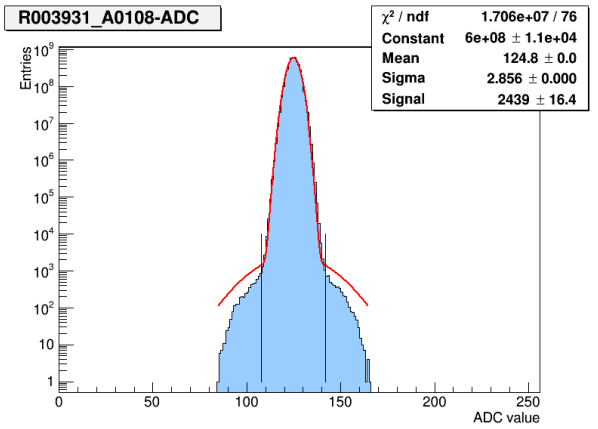
8 bit ADC range

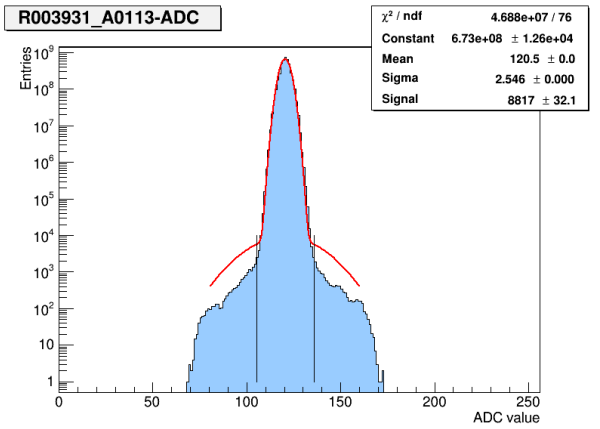


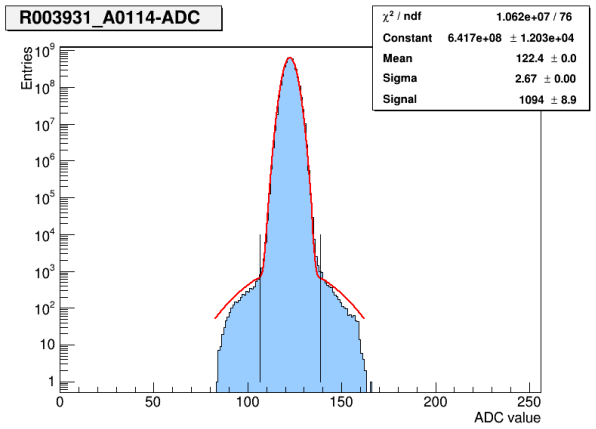
- Histogram of all ADC values
- Antenna 105
- Noise = 2 ADC counts
- All entries within 64 ADC counts
  - 6 bit range
- Signal / Noise
  - 6 for small hits (for 6 sigma thr)
  - Less than 40 for big hits
- 8 bits would be enough

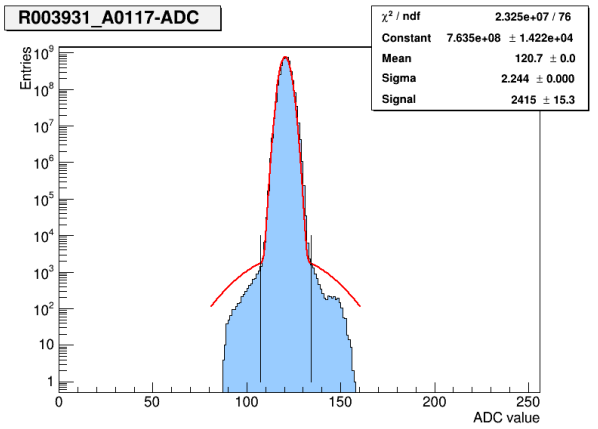
Other Examples

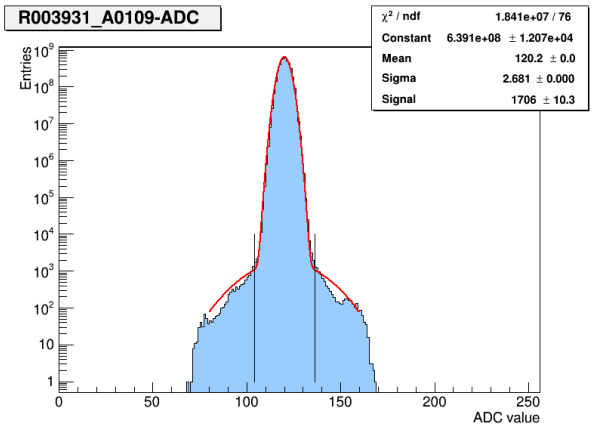




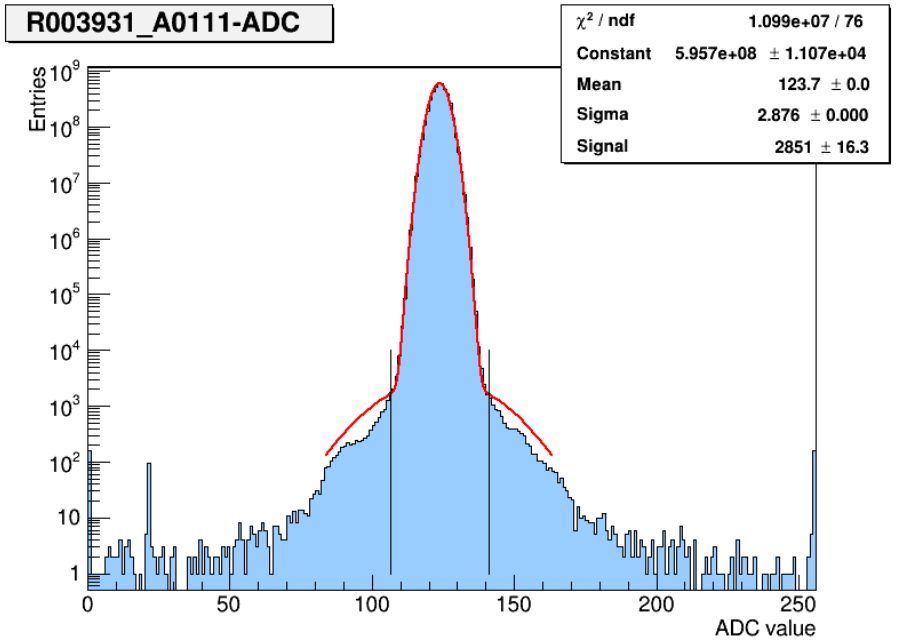






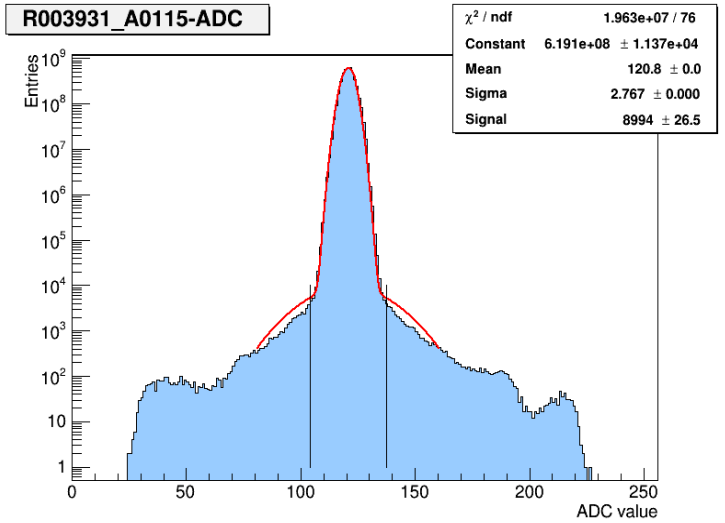


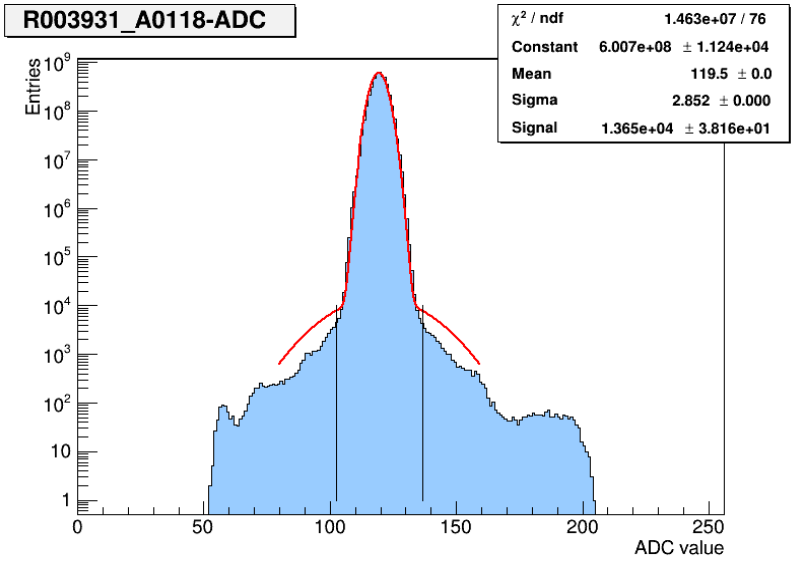
Antenna 111

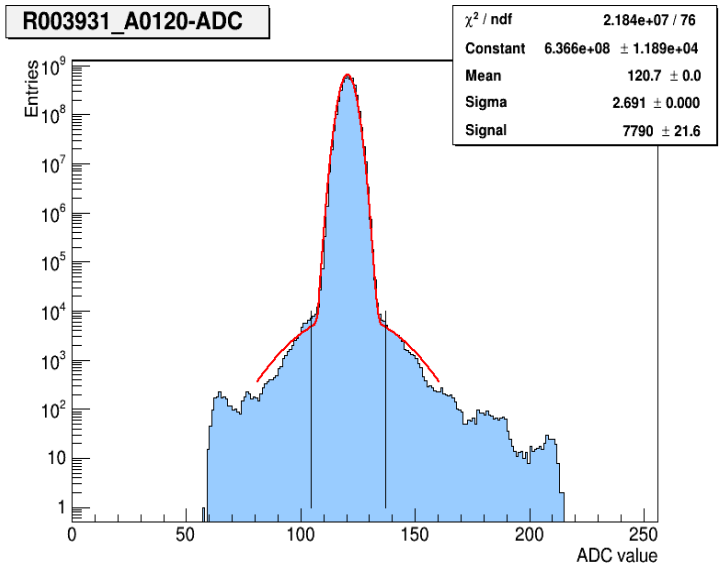


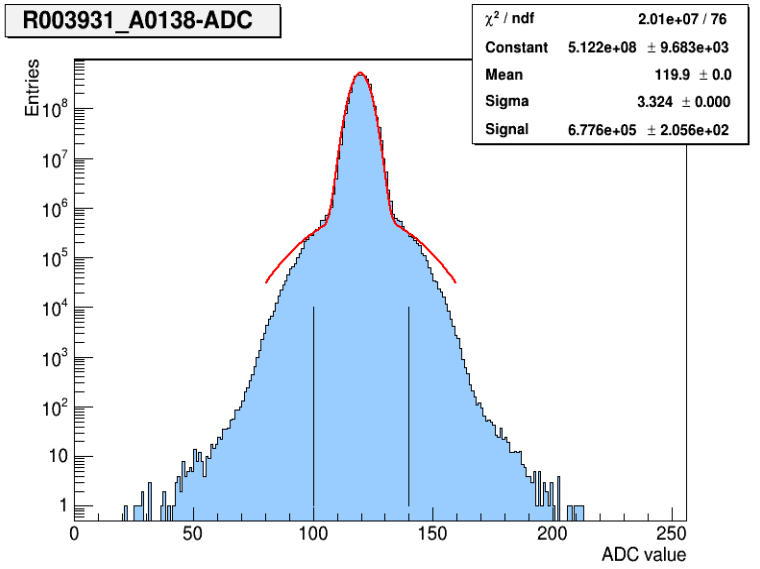
- Covers full range of 8 bits
- A few saturated entries
- Sigma = 2.9 ADC counts
  - Gain could be reduced
- Minimal loss, 8 bits still cover it well

Other examples









Virtual ribbon cable

- LHC uses the HDMP 1022/1024 chip set
  - 20 bits at 40 MHz ==> 0.8 GHz + protocol overhead
  - 15 years old and obsolete now
- We could use 4 bits at 200 MHz
  - Same data rate on fiber
  - Provides same clock to all antennas
  - Provides command and reset signals
- Otherwise, multiplexing a low rate data stream onto a clock signal could be done in the FPGA

Fiber: virtual ribbon cable