DAQ For TREND

version v1.0.4

Last modifications:

July 04, 2014:	Modification of different messages
July 07, 2014:	New ***TrendRdIntReg*** and ***TrendAck*** messages
August 25, 2014:	Modification of ***TRENDDAQ***: new bit (RdWrPlus)
August 28, 2014	New ***TRENDSlcReq*** message

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1. Introduction

This note describes the functionality of the new TREND electronics board.
This board is able to acquire the signal from 3-antenna. The interface with the central computer is done with the help of an fast Ethernet UDP link.

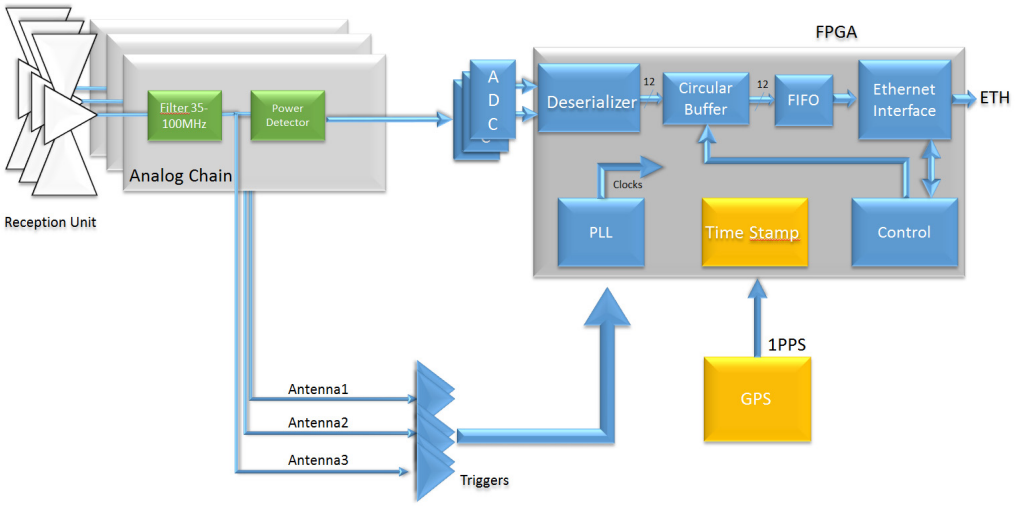

Figure 1.1: A general TREND synoptic

The figure 1.1 depicts the general TREND architecture. One reception unit is composed of 3-antenna. Each antenna is devoted to a particular direction (x,y,z). The analog chain is composed with a filter in the range 35-100MHz assuming noise reduction outside the useful bandwidth. A power detector is used to extract the signal envelop. A 12-bit 100MHz assumes the signal conversion.
A trigger logic with 6 comparators (2 comparators for each antenna, the signal can be positive or negative) fires when at least one comparator is above a programmable threshold. A trigger allows the digital part to acquire the data coming from the 3 ADC. The processed data are sent to Ethernet with a fast UDP protocol.
An ALTERA CYCLONE V 5CEFA4F23C6N FPGA controls all the board logic and the Ethernet communications with the central host. The UDP/Ethernet protocol is achieved using an optimized IP (Intellectual Property) core. This IP core is called GEDEK (Gigabit Data Exchange Kit) in this document.
The serial data coming from the ADCs are deserialized and written in a circular buffer. Whe na trigger is detected, a data block around the trigger time is sent into a FIFO and after on Ethernet.

2. Initial conditions

In order to work, a board must have an initial MAC and IP addresses. All the TREND boards are identical and at the power on, all the IP/MAC addresses are identical.
A dedicated chip (Dallas DS2502-48) located on the board provides a MAC address to the FPGA (figure 2.1). After a power on, the FPGA reads this unique 48-bit identifier from the Dallas chip. The DS2502-48 is compatible with the One-wire protocol. This MAC address is linked to the physical location.
In order to read correctly the DS2502-48 device, the FPGA must be compliant with the following sequence:

- Generate a Reset
- Detect the Presence bit

• Transfer the Read ROM command (33H)
• Read the data word: CRC (8-bit), ID=5E7H, SN (36-bit), Family Code=89

The MAC address will be deduce from ID&SN

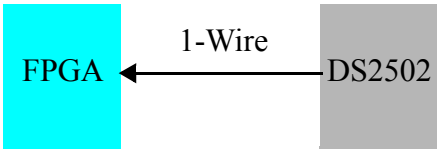

Figure 2.1: 1-Wire FPGA to DS2502 connection

A special procedure must be implemented to load the different IP addresses. This operation will be done in two steps in order to locate a board MAC Address in the set and to assign an IP address to a module:

• The first time, the system must address individually each port of each switch connected to the TREND module. In this situation, it is possible to associate an address MAC to a module and locating the MAC address in the set. This operation can take a long time but is done only one time.

• After a power off/on it is necessary to address each module with the RAW Socket protocol and thereafter program the corresponding IP Address. This operation is relatively fast.

3. Dynamic IP addressing

An option allows the dynamic IP addressing. This facility is useful to quickly switch between multiple data destinations, such as data acquisition and slow control data. In this case the MAC/IP destination addresses and PORT number are directly supply by the user to the GEDEK core.

4. Block structure

4.1. General block structure

It is important to define a block structure dedicated to the TREND DAQ.
All the data incoming or outgoing the FPGA are 32-bit words.
In the following document the terminology incoming message refers to data going from the control processing system to the FPGA. In the other hand, an outgoing message refers to data going from the FPGA to the control processing system.
2 message types are possible: the first one corresponds to a FPGA input and the second one to a FPGA output. In all the cases, a message is delimited by a Header and a Trailer.
In the following the Header and the Trailer are defined in hexadecimal as: AAAAAAA.
The *MSGTYPE* defines the type of the message and how to interpret the following data. The Data size depends on the *MSGTYPE*.
The table 4.1 shows an FPGA incoming message. In this case, the FPGA IP core decodes the IP address of the message.

Header	AAAAAAAA
MSGTYPE	
Data	
...	
Trailer	AAAAAAAA

Table 4.1: Message incoming the FPGA

In the case of an outgoing message, the structure is defined by the table 4.2.
The first word corresponds to MSGTYPE and defines how to interpret the data part. The third word defines the board address of the module and specifies the source of this message. This address corresponds to the IP address of the board. The size of the data block depends on the MSGTYPE.

Header	AAAAAAAA
MSGTYPE	
IP Address	
Data	
...	
Trailer	AAAAAAAA

Table 4.2: Message outgoing the FPGA

4.2. TRENDDAQ Message

Type: Incoming message.
This message defines the general DAQ parameters.

AAAAAAAA	[31:0] Header
00005000	[31:0] Message Type
0000[Offst][x][RdWrPlus][CalOn][DAQon]	[15:4][3][2][1][0]
AAAAAAAA	[31:0] Trailer

The *DAQon* bit allows setting the DAQ on or off. When in the off state the board is not able to capture any data.
When 0 the DAQ is off.
When 1 the DAQ is on.

CalOn allows disconnecting the input filter from the corresponding antenna and instead connect a 50 ohms resistor. This calibration mode allows testing the electronics without the antennas.
When 0 the input is in the normal mode connected to the antenna.
When 1 the input is connected to a 50 ohms resistor.
Ofst is a 12-bit word defining the offset in the circular memory. When a trigger fires when writing the Current Address (*CA*), all the words between *CA-offset* and *CA+offset-1* will be read by the FPGA (figure 4.1).

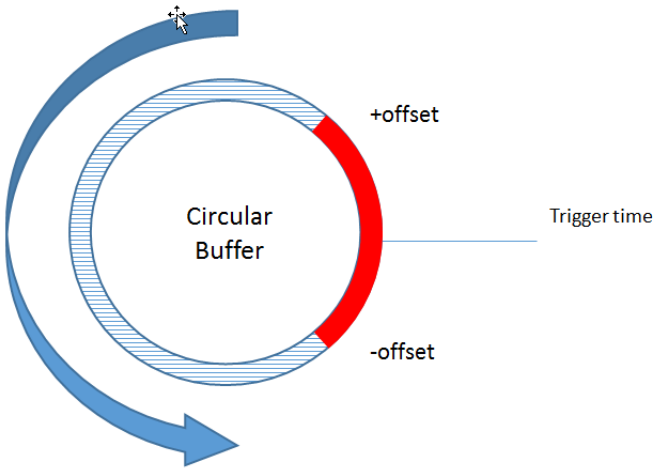

Figure 4.1: The circular buffer and the offset

RdWrPlus=1 specifies that the circular buffer is in the write/read simultaneous mode. When *RdWrPlus*=0, the read and the write operations are sequential.
In this case, the sequence is the following: the circular buffer is in writing mode.When a trigger arrives the system continues writing Offset words then the writing stops and the read sequence occurs.
RdWrPlus=1 allows reducing the dead time of the quantity of offsetx10ns.

4.3. TRENDTRIG Message

Type: Incoming message.
This message defines the different trigger parameters. All the message words are 32-bit.

AAAAAAAA	[31:0] Header
00005100	[31:0] Message Type
[TrgEn][ST]	[6:1][0]
[Th1+][Th1-]	[23:12][11:0]
[Th2+][Th2-]	[23:12][11:0]
[Th3+][Th3-]	[23:12][11:0]
AAAAAAAA	[31:0] Trailer

ST bit is the soft trigger command, when ’1’ a soft trigger is sent and a data block captured.
TrgEn is 6-bit word defining which trigger channel are active. A *TrgEn* bit is dedicated to each trigger channel (figure 4.2).
When all the *TrgEn* bits are set to ’0’, the DAQ is disabled.
Thi+ is the positive comparator threshold (12-bit) with *i*=1,2 or3.
Thi- is the negative comparator threshold (12-bit) *i*=1,2 or3.
With *i* referring to the antenna number (*i*=1,2, or3).

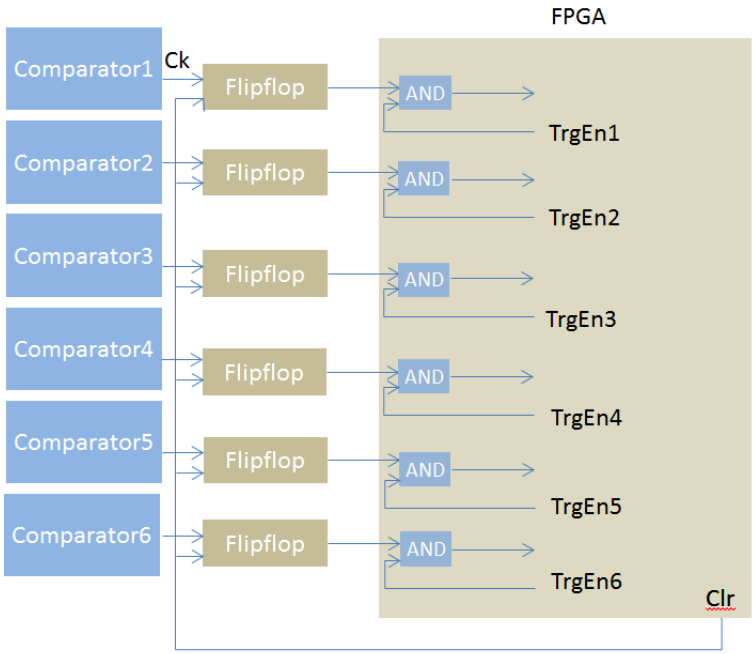

Figure 4.2: Trigger control

4.4. TRENDSlcReq Message

Type: Incoming message.
TRENDSlcReq is used to request a ***TRENDSLC*** message including the slow control reading.

AAAAAAAA	[31:0] Header
00005200	[31:0] Message Type]
AAAAAAAA	[31:0] Trailer

4.5. TRENDIntReg Message

Type: Incoming/outgoing message.
TRENDIntReg is used to program the IP/MAC/PORT registers.
It is also possible to dynamically insert for each frame a new IP/MAC/PORT destination addresses. For the TREND project it is interesting to switch between two sets of destination addresses. The first set will be dedicated to the data and the second to the slow control.
AD0 to AD4 are compatible with the non-dynamic IP/MAC/PORT destination addresses. In this case, theses values are written in the *GEDEK* core.

TRENDIntReg Y=0

AAAAAAAA	[31:0] Header
00005E00	[31:0] Message Type]
0000000Y	Y=0 read back
AAAAAAAA	

TRENDIntReg Y=1

AAAAAAAA
00005E00
0000000YY=1 write the following registers, Y=0 read back
AD0FPGA Board MAC Address (32 LSB)
AD1FPGA Board IP Address (32 LSB)
AD2Destination MAC1 Address (32 LSB)
AD3Destination MAC1 Address (16 MSB)
AD4Destination IP1 Address (32 LSB)
AD5Destination MAC2 Address (32 LSB)
AD6Destination MAC2 Address (16 MSB)
AD7Destination IP2 Address (32 LSB)
AD8Destination PORT1 (16 LSB)
AD9Destination PORT2 (16 LSB)
AAAAAAAA

When a read request for the internal registers is received, a new MAC address read is initiated on the 1-Wire bus and the internal *GEDEK* registers are read back (**TrendIntRdReg**).

4.6. TrendData Message

Type: Outgoing message.
The ***TrendData*** Message is used for transferring the acquisition data to the central processing system.

AAAAAAAA	[31:0] Header
00005A00	[31:0] Message Type
IP Num	[31:0] Board IP Address
[TS2]	[31:0] Time stamp 0
[**0**][TS1PPS][TS1Trigger]	[31:16][15:8][7:0] Time stamp 1
[**0**][TrigPattern]	[31:6][5:0] Trigger Pattern
[**0**][Data1][Data0]	[31:24][23:12][11:0] Antenna 1
[**0**][Data3][Data2]	[31:24][23:12][11:0] Antenna 1
....	
[**0**][Data(2offset-1)][Data(2offset-2)]	[31:24][23:12][11:0] Antenna 1
[**0**][Data1][Data0]	[31:24][23:12][11:0] Antenna 2
[**0**][Data3][Data2]	[31:24][23:12][11:0] Antenna 2
....	
[**0**][Data(2offset-1)][Data(2offset-2)]	[31:24][23:12][11:0] Antenna 2
[**0**][Data1][Data0]	[31:24][23:12][11:0] Antenna 3
[**0**][Data3][Data2]	[31:24][23:12][11:0] Antenna 3
....	
[**0**][Data(2offset-1)][Data(2offset-2)]	[31:24][23:12][11:0] Antenna 3
AAAAAAAA	[31:0] Trailer

A set of three data block are sent (one data block correspond to the data of an antenna).
For each antenna the data block size is 2xOffset, so for 3 antennas the global data block size is 6xOffset. In a 32-word it is possible to pack 2-antenna words [Datai+1][Datai]. Each [Datai] is a 12-bit word. The upper part of each 32-bit Data word [31:24] is set to 0.

The TREND system allows to time stamp each trigger relatively to the 1PPS reference signal. This time stamping is composed of 2-word *TS1* and *TS2*.
TS1 is a 32-bit counter specifying the number of 8ns slots between the 1PPS signal and the trigger signal.
TS2 is composed of 2-8bits words. the first one, *TS1Trigger* time stamps the Trigger inside the 8ns slot. *TS1PPS* gives the phase of the 1PPS inside the 8ns slot.

TrigPattern is the pattern trigger state when the comparator fires.

4.7. TrendSlc Message

Type: Outgoing message.
The ***TrendSlc*** message allows reading the slow control parameters of the TREND board.

AAAAAAAA	[31:0] Header
00005B00	
IP Num	
[**0**]VPower1	[31:12][11:0]
[**0**]VPower2	[31:12][11:0]
[**0**]VPower3	[31:12][11:0]
[**0**][Th1+][Th1-]	[31:24][23:12][11:0]
[**0**][Th2+][Th2-]	[31:24][23:12][11:0]
[**0**][Th3+][Th3-]	[31:24][23:12][11:0]
[**0**][Temp]	[31:12][11:0]
[**0**][Hygro]	[31:12][11:0]
AAAAAAAA	[31:0] Trailer

VPower1,2,3 are the monitoring of different important voltages of the board. These voltages are

read back with a 12-bit ADC.
Thi+ and *Thi-* are the reading back of the trigger thresholds written with the ***TRENDTRIG*** message.

4.8. TrendRdIntReg Message

Type: Outgoing message.
The ***TrendRdIntReg*** block is sent by the FPGA after a ***TRENDIntReg*** request, the internal registers are sent to the host.

AAAAAAAA	
00005C00	
IPNum	[31:0]
Board MAC Ad.	[31:0] (LSB)
Board IP Ad.	[31:0]
Dest. MAC1 Ad.	[31:0] (LSB)
[**0**][Dest. MAC1 Ad.]	[31:16][15:0] (MSB)
Dest IP1 Ad.	[31:0]
Dest. MAC2 Ad.	[31:0] (LSB)
[**0**][Dest. MAC2 Ad.]	[31:16][15:0] (MSB)
Dest IP2 Ad.	[31:0]
[**0**][Dest Port1]	[31:16][15:0]
[**0**][Dest Port2]	[31:16][15:0]
Serial Number	[31:0] (LSB)
Serial Number	[31:0] (MSB)
AAAAAAAA	

In this block *IPNum* is identical to Board IP Ad.
Each FPGA as an embedded unique 64-bit serial number. This number is included in the outgoing ***TrendRdIntReg*** message.
The destination MAC Address (MAC1 ans MAC2) are 48-bit words. In the previous block these values are splited in 2 words, the LSB is 32-bit and the MSB part is 16-bit. In this case the upper part of the MSB is [31:16]=0000H.

4.9. TrendACK Message

Type: Outgoing message.
All the incoming slow control messages are acknowledged by a specific ***TrendACK*** Message.

AAAAAAAA	
00005D00	
IP Num	[31:0]
[**0**][MsgAck]	[31:16][15:0]
AAAAAAAA	

With *MsgAck* the message type to acknowledged. The *MsgAck* field is [15:0], the upper part of the 32-bit word is [31:16]=0000H.

5. Messages summary

The table 5.1 summarizes all the TREND messages.

Message	Code (Hex)	Direction
TRENDDAQ	5000	incoming
TRENDTRIG	5100	incoming
TRENDSlcReq	5200	incoming
TRENDIntReg	5E00	incoming
TRENDData	5A00	outgoing
TRENDSlc	5B00	outgoing
TrendRdIntReg	5C00	incoming/outgoing
TrendACK	5D00	outgoing

Table 5.1: TREND Messages summary